REMARKS

Status Summary

Claims 1–25 are pending in the present application. Claims 1, 11, 14 and 23 presently stand rejected, and claims 2–10, 12, 13, 15–22, 24 and 25 have been objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 11 and 23 has been amended. New claim 26 has been added. No new matter has been introduced by the present amendment. Reconsideration of the application as amended and based on the arguments set forth herein below is respectfully requested.

Specification

The Examiner has stated that the abstract should be a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains, should include the technical disclosure of the improvement, and should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. The abstract has been amended as indicated above.

Claim Rejection - 35 U.S.C. § 102

Claims 1, 11, 14 and 23 stand rejected by the Examiner under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,647,076 to Schenk et al., hereinafter referred to "Schenk", which is recognized as prior art in the introductory

portion of the present application and is extensively discussed with respect to Figure 5 of the present application. With regard to claim 1, the Examiner contends that Schenk discloses a circuit arrangement for compensating for disturbances in a signal generated by means of a discrete multitone modulation comprising: a multiplicity of first adder circuits, the multiplicity of first adder circuits being supplied with a first error signal vector and the multiplicity of first adder circuits adding the first error signal vector to at least one first signal vector in order to generate an error-corrected first signal vector; and a multiplicity of first multiplier circuits which precede the multiplicity of first adder circuits and multiply the first error signal vector by adjustable coefficients wherein the first error signal vector is a signal vector of a carrier frequency which is not used for transmitting data via the transmission channel.

With regard to claim 11, the Examiner further contends that Schenk discloses a circuit arrangement for compensating for disturbances in a signal generated by means of a discrete multitone modulation comprising: decision circuits which are in each case supplied with a reference signal vector and which map the respective reference signal vector into a respective value-discrete reference signal vector; subtracting circuits for forming a respective error signal vector which subtract the respective reference signal vector and the respective value-discrete reference signal vector from one another; groups of first adder circuits, each group of first adder circuits in each case being supplied with an error signal vector and the groups of first adder circuits adding the respective error signal vector to at least one signal vector in order to generate a progressively error-corrected signal vector; and groups of first

multiplier circuits which in each case precede a group of first adder circuits and multiply the respective error signal vector by adjustable coefficients.

With regard to claim 14, the Examiner additionally contends that Schenk discloses a method for compensating for disturbances in a signal generated by means of discrete multitone modulation comprising the following steps: multiplying at least one error signal vector by adjustable coefficients; and adding the at least one error signal vector multiplied by the adjustable coefficients to at least one signal vector in order to generate an error-corrected signal vector, wherein the at least one error signal vector is a signal vector of a carrier frequency which is not used for transmitting data via the transmission channel.

With regard to claim 23, the Examiner contends that Schenk discloses a method for compensating for disturbances in a signal generated by means of discrete multitone modulation comprising the following steps: mapping a respective reference signal vector into a respective value-discrete reference signal vector; subtracting the respective reference signal vector and the respective value-discrete reference signal vector from one another in order to form a respective error signal vector; multiplying the respective error signal vector by adjustable coefficients; and adding the respective error signal vector multiplied by the adjustable coefficients to at least one signal vector in order to generate a progressively error-corrected signal vector.

The positions of the Examiner as summarized above with respect to claims 1, 11, 14 and 23 are respectfully traversed as described below.

With regard to claims 1 and 14, the Applicant respectfully disagrees with the evaluation of Schenk by the Examiner. Specifically, the last element of both claims 1 and 14 recite that either the first error signal vector or at least one error signal vector is a signal vector of a carrier frequency which is not used for transmitting data via the transmission channel. This characteristic of the claimed subject matter is not disclosed by Schenk, which teaches to use reference signal vectors with reference frequency channels that are used for data transmission. The reference signal vector $\mathbf{a_0}$, $\mathbf{b_0}$ disclosed by Schenk is merely "an arbitrary signal vector" selected from among the multiplicity of signal vectors that are all used for data transmission. (See, e.g., Col. 5, lines 42–44; Col. 5, line 61 through Col. 6, line 8)

Because of this data transmission and, therefore, because of the modulation of the frequency channel for a reference signal, the arrangement and method disclosed by Schenk requires a frequency equalizer **30**, a decision circuit **40**, and subtracting circuits **6**, **7** for creating the real part $\Delta\mathbf{a_0}$ and the imaginary part $\Delta\mathbf{b_0}$ of the error signal vector. In contrast, the arrangement and method of pending claims 1 and 14 dispense with frequency domain equalizers, decision circuits, and subtracting circuits for the reference frequency channel that is not used for data transmission.

This difference is also clearly indicated in Figures 1–4 of the present application, and in particular, is illustrated through the signals $\mathbf{a_r}$ and $\mathbf{b_r}$ forming the respective reference signal vector. According to the pending claims, the error signal vector $\mathbf{a_r}$, $\mathbf{b_r}$ is directly withdrawn from the demodulator **2**, fed through multiplier circuits **14** for multiplying with adjustable coefficient, and finally provided to adder

circuits **18**, **19** for adding the multiplied error signal vector components to signal vectors used for data transmission. This arrangement provides that an error signal vector is a signal vector of a carrier frequency which is not used for transmitting data via the transmission channel. This feature is neither taught nor suggested by Schenk, and, accordingly, it is respectfully submitted that claims 1 and 14 are in proper condition for allowance.

With regard to claims 11 and 23, the Applicant also respectfully disagrees with the evaluation of Schenk by the Examiner. Claims 11 and 23 disclose the progressive error correction achieved by adding more than one error signal vector to a signal vector whose signal quality is to be improved, and claims 11 and 23 have been amended to emphasize this feature. Specifically, presently pending claim 11 recites "more than one group of first adder circuits, each group of first adder circuits in each case being supplied with an error signal vector and the groups of first adder circuits adding the respective error signal vectors to each of at least one signal vector in order to generate a progressively error-corrected signal vector." Likewise, presently pending claim 23 recites the step of "adding the plurality of respective error signal vectors multiplied by the adjustable coefficients to each of at least one signal vector in order to generate a progressively error-corrected signal vector." The cited reference Schenk expressly teaches to employ one single reference signal vector (e.g., $\mathbf{a}_0$, $\mathbf{b}_0$ in Fig. 1 of Schenk) for generating one single error signal vector ($\mathbf{a'}_0$, $\mathbf{b'}_0$) that is to be added to the chosen signal vector to be improved ($\mathbf{a}_n$, $\mathbf{b}_n$). Accordingly, Schenk does not teach or suggest using a plurality of error signal vectors being

added to one signal vector for generating the progressively error-corrected signal vector.

By increasing the number of reference channels or error signal vectors, respectively, the residual error in the signal vectors used for data transmission can be further reduced. The error compensation according to the present invention and claimed in claims 11 and 23 achieves better results than taught by Schenk. (See, page 11, lines 15-25 of specification as filed) Generally, a transmission channel including transmitting and receiving filters cannot be described by a second order transfer function, or the recovery of said channel cannot be described by a second order linear differential equation with constant coefficients. Hence, a residual error remains when employing a strategy as illustrated in Figure 5 of the present application or the method and apparatuses as disclosed in Schenk. Progressively error-corrected signal vectors according to claims 11 and 23, however, are less influenced by residual errors due to the recovery of the transmission channel. This feature is neither taught nor suggested by Schenk, and, accordingly, it is respectfully submitted that claims 11 and 23 are in proper condition for allowance.

New Claims

New claim 26 has been added by this amendment as indicated above.

Claim 26 is an independent claim reciting a circuit arrangement for compensating for disturbances in a signal generated by means of discrete multitone modulation (DMT), the signal generated by means of discrete multitone modulation

exhibiting in the frequency domain a multiplicity of carrier frequencies which are used for transmitting data via a transmission channel, and each carrier frequency exhibiting a signal vector. The circuit arrangement comprises decision circuits which are in each case supplied with a reference signal vector and which map the respective reference signal vector into a respective value-discrete reference signal vector; subtracting circuits for forming a respective error signal vector which subtract the respective reference signal vector and the respective value-discrete reference signal vector from one another; a multiplicity of first adder circuits, the multiplicity of first adder circuits in each case being supplied with an error signal vector from an adjacent carrier frequency and the multiplicity of first adder circuits adding the respective adjacent error signal vector to at least one signal vector in order to generate an error-corrected signal vector; and a multiplicity of first multiplier circuits which in each case precede the multiplicity of first adder circuits and multiply the respective adjacent error signal vector by adjustable coefficients.

It is respectfully submitted that new claim 26 is allowable over the prior art. No new matter is considered to have been added.

CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above Remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

DEPOSIT ACCOUNT

A check is submitted with this amendment for the fee for adding a new independent claim.

The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

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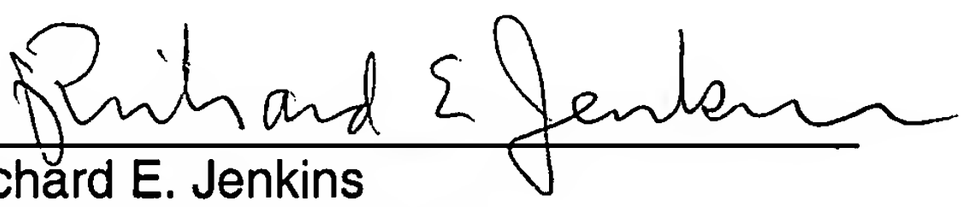
Date: August 1, 2007 By: 

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